A Pseudo 2D Analysis Of The Velocity Saturation Region For Flash Cell Modeling

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Introduction

Flash cell is the most important non volatile memory because of its high integration density and high speed. Programming Flash cells uses the channel hot electron current injection mode which occurs in the velocity saturation region (VSR). Since, the electric field in the VSR region is two dimensional, a pseudo 2D analysis is necessary, especially for new technologies generation.

We proposed an analytical drift-diffusion surface-potential-based model for metal oxide semiconductor (MOS) transistor operating in the saturation region. The two-dimensional nature of the region near the drain of this transistor is considered. This pseudo-2D analysis of the saturated region allows the determination of the spatial repartition along the saturated channel of the surface potential and the electrical field. This new MOS model is integrated in a compact floating gate memory model of Flash [1] to evaluate the drain current, substrate current and the channel hot electron for the writing operation.

Pseudo 2D analysis of the VSR region

The proposed model is based on two-sections approach that consists of dividing the channel length, when the MOS is operating in saturation regime, into two regions. The first one is the source region , which extends from the source to the saturation point, where the Gradual Channel approximation (GCA) is valid. The second is the velocity region where the carrier velocity is saturated and the problem becomes 2D in nature and then the GCA fails.

The current in the linear regime is given by the drift-diffusion surface-potential-based model [2] in which a novel mobility law is integrated to improve the model accuracy. The drain current is evaluated by the calculation of the surface potential at the boundary of the GCA channel. The current in the saturated regime is given by assuming a constant charge and a saturated velocity.

To evaluate the position of the saturation point and its surface potential a pseudo 2D analysis of the velocity saturation region is done. This pseudo 2D analysis is based on the approach proposed by El-Mansy [3]. An improvement of this pseudo-2D approach is proposed concerning the saturation point definition as well as the Gauss volume and the lateral electrical field dependence on coordinates (x, y). The saturation point is defined in this model such as the point of channel at which the saturation velocity is reached. This definition is improved by taking into account the potential variation, at this point, with V_{DS}. The proposed Gauss's volume as illustrated in continuous lines in Fig. 1 is more complete compared to the one assumed by El-Mansy (dotted lines). In fact, it is limited by the depleted zone boundary. The potential in the saturated region is assumed function of x and y.

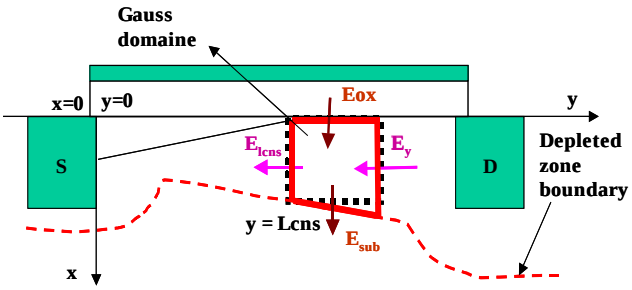

Fig. 1: Schematic cross-section of a MOS transistor the saturation regime

The application of the Gauss theory and the differentiation of the obtained equation with respect to *y*, with the assumption of a constant mobile charge within the saturated channel, leads to a second order differential equation of the surface potential. The resolution of this equation leads to the evaluation of the surface potential and the lateral electric field along the saturated channel.

The evaluation of surface potential at the drain gives the length of the velocity saturation region. The condition of the current continuity at the transition linear/saturated regime gives the length of the non saturated region.

These two lengths are function of the saturation surface potential ψ_{sat} which is unknown. Since, their sum is equal to the effective canal length, ψ_{sat} is then the potential that leads to this equality. This parameter is computed by dichotomy.

Conclusion

We have developed a pseudo 2D analysis of the velocity saturation region, using an analytical drift-diffusion surface-potential-based model, which is integrated in a compact floating gate memory model. This one can be used to analyse the cell electrical behaviour in order to improve cell design and also to create some new memories structures. With this model, we can simulate both transient and static characteristics.

A validation of the model is performed on transistors MOS and on Flash memory cell.

References

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